EXHIBIT A

PATENT
Atty. Dkt. No. 121-0019-US-REG

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Andrew WOLFE	§	
	§	Group Art Unit: 2115
Serial No.: 12/713,220	§	
Confirmation No.: 4243	§	
	§	Examiner: BUTLER, DENNIS
Filed: February 26, 2010	§	
For: PROCESSOR CORE COMMUNICATION IN MULTI-CORE PROCESSOR	§	

MAIL STOP AMENDMENT
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

RESPONSE TO OFFICE ACTION DATED AUGUST 29, 2012

In response to the non-final Office Action dated August 29, 2012 having a shortened statutory period for response set to expire on November 29, 2012, please enter this response and reconsider the claims pending in the application for the reasons discussed below. Although Applicant believes that no fees are due in connection with this response, the Commissioner is hereby authorized to charge Counsel's Deposit Account No. 50-4588/121-0019-US-REG for any fees, including extension of time fees or excess claims fees, required to make this response timely and acceptable to the Office.

Amendments to the Specification are reflected on page 2 of this paper. **Amendments to the Claims** are reflected in the listing of claims which begins on page 3 of this paper. **Remarks** begin on page 8 of this paper.

IN THE CLAIMS:

The listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A multi-core processor, comprising:

a first set of processor cores of the multi-core processor, wherein each processor core from the first set of processor cores is configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (PLL) having a first clock signal as input;

a second set of processor cores of the multi-core processor, wherein each processor core from the second set of processor cores is configured to dynamically receive a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal; and

an interface block coupled to the first set of processor cores and also coupled to the second set of processor cores, wherein the interface block is configured to facilitate communication between the first set of processor cores and the second set of processor cores.

2. (Original) The multi-core processor of claim 1, the interface block further comprising a first level shifter that is referenced to the second supply voltage and adapted to translate first logic levels associated with the first set of processor cores to second logic levels associated with the second set of processor cores for a first signal traveling from the first set of processor cores to the second set of processor cores.

3. (Original) The multi-core processor of claim 1, the interface block further comprising a second level shifter that is referenced to the first supply voltage and adapted to translate second logic levels associated with the second set of processor cores to first logic levels associated with the first set of processor cores for a second signal traveling from the second set of processor cores to the first set of processor cores.

4. (Original) The multi-core processor of claim 1, wherein the interface block further comprises a synchronizer configured to synchronize the first clock signal and the second clock

REMARKS

This is intended as a full and complete response to the Office Action dated August 29, 2012, having a shortened statutory period for response set to expire on November 29, 2012. By way of this reply, Applicant is amending claims 1, 10-11, 15, and 18-23. Claims 1 – 23 are pending. Applicant is also amending paragraph [0017] in the as filed application, which describes FIG. 4, to correct typographical errors. No new matter has been added.

Examiner Interview

Applicant thanks Examiner Butler for the November 27, 2012 telephone interview. The interview included discussions of the 35 U.S.C. § 101 rejections, 35 U.S.C. § 112 rejections, 35 U.S.C. § 102, and 35 U.S.C. § 103 rejections in view of the references cited in the Office Action. An agreement was reached regarding the 35 U.S.C. § 101 rejections and the 35 U.S.C. § 112 rejections. Pending the Examiner's further searches, the Examiner acknowledges that the architecture shown and described in the present disclosure differs from the currently cited references.

Applicant respectfully submits that the claims as presented in this response substantially reflect the discussions during the interview.

Claim Objections

Claims 22 – 23 are objected to under 37 CFR 1.75 as allegedly being substantial duplicates of claims 10 and 11. Claims 22 – 23 have been amended to depend on claims 21 and 22, respectively. Claim 21 also recites different elements than claim 1 (e.g., a power control block and a clock control block). Applicant respectfully requests the withdrawal of the claim objections.

35 U.S.C. § 101 Rejection

Claims 18 – 20 are rejected under 35 U.S.C. §101, because the claimed invention is allegedly directed to non-statutory subject matter. The suggested "non-transitory" language has been added, and Applicant respectfully requests the withdrawal of the rejections under 35 U.S.C. §101.

35 U.S.C. § 112 Rejection

Claims 15 – 20 are rejected under 35 U.S.C. §112, second paragraph for being allegedly indefinite and failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. As discussed during the interview, Applicant has amended

independent claims 15 and 18 to clarify that the communication is "between the first set of processor cores and the second set of processor cores." The amendments are at least supported by paragraph [0018] and FIG. 1, FIG. 3, and FIG. 4 of the as filed application. Applicant respectfully requests the withdrawal of the rejections under 35 U.S.C. §112.

35 U.S.C. § 102 Rejections

Claims 1, 5 – 6, 8 – 9, 14 and 21 are rejected under 35 U.S.C. §102(e) as being allegedly anticipated by U.S. Patent Application Publication 2009/0106576 (hereinafter *Jacobowitz*).

Applicant does not concede that the above reference is prior art and reserves the right to challenge the reference at a later date. Further, Applicant respectfully submits that the rejections are overcome for at least the reasons stated below.

To anticipate a claim, the alleged reference must teach each and every element of the claim. Applicant respectfully submits that *Jacobowitz* does not teach or suggest one or more elements of the amended independent claims 1 and 21. Specifically, *Jacobowitz* does not teach or suggest at least the elements of "a first set of processor cores… configured to dynamically receive a first supply voltage and a first output clock signal of a first phase lock loop (LLP) having a first clock signal as input," "a second set of processor cores… configured to dynamically received a second supply voltage and a second output clock signal of a second PLL having a second clock signal as input, wherein the first supply voltage is independent from the second supply voltage, and the first clock signal is independent from the second clock signal." The claim amendments are at least supported by paragraph [0015] and FIG. 3 of the as filed application.

First, *Jacobowitz* fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first supply voltage and a second supply voltage, respectively. In addition, the first supply voltage is independent from the second supply voltage, as required in the amended independent claims 1 and 21. Paragraph [0043] of *Jacobowitz* merely mentions that "[f]urther power management can be realized by controlling the power supply voltage (Vdd) to each core and/or chip." In other words, *Jacobowitz* is silent with respect to least the recited different sets of processor cores configured to receive independent supply voltages.

Second, FIG. 6 and all other figures of *Jacobowitz* clearly show that the microprocessor chip (e.g., 600) receives a system reference oscillator clock frequency (v_R) and distributes v_R to local oscillators 108. See *Jacobowitz*, paragraphs [0037]-[0038] and FIG. 6. *Jacobowitz* fails to

disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal as input, respectively. In addition, the first clock signal is independent from the second clock signal, as required in the amended independent claims 1 and 21.

For at least the reasons set forth above, the amended independent claims 1 and 21 and the related dependent claims 2 – 14 and 22 – 23 are patentable over *Jacobowitz*. Applicant respectfully requests the withdrawal of the rejections under 35 U.S.C. §102.

35 U.S.C. § 103 Rejections

Claims 2 – 4, 7, 12 and 13 are rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over *Jacobowitz* in view of U.S. Patent Application Publication 2009/0138737 (hereinafter *Kim*).

Claims 10 – 11, 15 – 20 and 22 – 23 rejected under 35 U.S.C. §103(a) as being allegedly unpatentable over *Jacobowitz* in view of Kim and further in view of U.S. Patent Application Publication 2010/0188115 (hereinafter *von Kaenel*).

Applicant does not concede that the aforementioned references are prior art and reserves the right to challenge these references at a later date. Further Applicant respectfully submits that these rejections are overcome for at least the reasons stated below.

To establish a *prima facie* case of obviousness required for a §103(a) rejection, the references must teach or suggest all the claim elements.

Claims 2 – 4, 7, 12 and 13

As discussed during the interview, *Kim* discloses a different architecture than the one recited in the present disclosure. Specifically, as shown in FIG. 1 and FIG. 2 of *Kim*, *Kim* fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first supply voltage and a second supply voltage, which is independent from the first supply voltage, respectively. Instead, *Kim* discloses having each core, not a set of processor cores, received a V_{DD} (i.e., V_{DD1}, V_{DD2}, V_{DD3}, and V_{DD4}).

In addition, *Kim* also fails to disclose or teach a first set of processor cores and second set of processor cores configured to dynamically receive a first output clock signal of a first PLL having a first clock signal as input and a second output clock signal of a second PLL having a second clock signal, respectively. In addition, the first clock signal is independent from the second clock signal. Instead, *Kim* discloses the apparatus comprising a multi-core processor (i.e., 100 in FIG. 1 or 200 in FIG. 2) having a single clock source (i.e., 170 in FIG. 1 or 270 in

CONCLUSION

Having addressed all issues set out in the office action, Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that the claims be allowed. If there are any questions about any of the foregoing, please contact Applicant's undersigned representative.

Respectfully submitted,

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